IN THE CLAIMS

1. (Currently amended) A multi-chip module comprising:

a substrate having a plurality of interconnections formed on a top surface thereof;

a lowest chip and at least one top chip sequentially stacked on the top surface, the top chip having an insulating tape attached to a backside thereof, the lowest chip and the top chip each having pads formed thereon;

an insulator interposed between the chips, the insulator exposing the pads; and

a first group of bonding wires connecting the pads of the lowest chip with a first group of interconnections on the substrate, wherein the insulating tape attached to the backside of the top chip insulates the first group of bonding wires from contacting or connecting to any part of the top chip.

2. (Original) The multi-chip module of claim 1, further comprising:

a second group of bonding wires connecting the pads of the top chip with a second group of interconnections on the substrate.

3. (Original) The multi-chip module of claim 1 wherein all the chips have substantially the same dimension and fully cover each other.

4. (Original) The multi-chip module of claim 1 wherein the top chip has a greater planar area than the lowest chip located thereunder.

5. (Original) The multi-chip module of claim 1 further comprises an adhesive interposed between the lowest chip and the substrate.

6. (Original) The multi-chip module of claim 1 further comprises bumps formed on the pads of the chips, the bonding wires being in contact with the bumps.

7. (Original) The multi-chip module of claim 1 further comprises an epoxy molding compound that encapsulates the stacked chips and the bonding wires.

8. (Original) The multi-chip module of claim 1 wherein the lowest chip and the top chip each have peripheral pads formed on a top surface thereof.

9. (Original) The multi-chip module of claim 1 wherein the insulator has a smaller width than the chips to expose the pads.

10. (Currently amended) A multi-chip module comprising:

a substrate having a plurality of interconnections formed on a top surface thereof, the interconnections including a first group of interconnections and a second group of interconnections;

a bottom chip and a top chip sequentially stacked on the top surface, the top chip having an insulating tape attached to its backside and the bottom chip and the top chip each having peripheral pads on a top surface thereof;

an insulator interposed between the bottom chip and the top chip, the insulator having a smaller width than the chips to expose the pads of the bottom chip;

a first group of bonding wires connecting the pads of the bottom chip with the first group of interconnections, wherein the insulating tape attached to the backside of the top chip insulates the first group of bonding wires from contacting or connecting to any part of the top chip; and

a second group of bonding wires connecting the pads of the top chip with the second group of interconnections.

11. (Original) The multi-chip module of claim 10 wherein the substrate is a lead frame or a printed circuit board.

12. (Currently amended) The multi-chip module of claim 11[[10]] wherein the top chip has substantially the same dimensions as the bottom chip.

13. (Original) The multi-chip module of claim 10 wherein the top chip has a greater planar area than the bottom chip.

14. (Original) The multi-chip module of claim 10 further comprises an adhesive interposed between the bottom chip and the substrate.

15. (Currently amended) The multi-chip module of claim 12[[10]] further comprises conductive bumps formed on the pads of the chips, the bonding wires being in contact with the bumps.

16. (Currently amended) The multi-chip module of claim 15[[10]] further comprises an epoxy molding compound that encapsulates the bottom chip, the top chip and the bonding wires.

17. (Currently amended) A method of fabricating a multi-chip module, the method comprising:

preparing a substrate having first and second groups of interconnections formed on a top surface thereof;

mounting a bottom chip on the top surface, the bottom chip having pads formed thereon;

forming a first group of bonding wires that connect the pads of the bottom chip to the first group of interconnections;

attaching an insulator on an upper surface of the bottom chip, the insulator being surrounded by the pads of the bottom chip; ~~and~~

adhering an insulating tape to a backside of a top chip; and

mounting the[[a]] top chip on the insulator, ~~the top chip including an insulating tape attached to a backside thereof, and~~ the top chip having pads formed thereon.

18. (Original) The method of claim 17 further comprising:

forming a second group of bonding wires that connect the pads of the top chip to the second group of interconnections.

19. (Original) The method of claim 17 further comprises providing an adhesive on the substrate before mounting the bottom chip on the substrate, the bottom chip being fixed to the substrate by the adhesive.

20. (Original) The method of claim 17 further comprises forming bumps on the pads of the bottom chip before forming the first group of bonding wires, the first group of bonding wires being connected to the bumps on the pads of the bottom chip.

21. (Original) The method of claim 20, wherein the first group of bonding wires are formed using a bump reverse bonding technique.

22. (Original) The method of claim 17 further comprises forming bumps on the pads of the top chip before forming the second group of bonding wires, the second group of bonding wires being connected to the bumps on the pads of the top chip.

23. (Original) The method of claim 17 further comprises forming an epoxy molding compound that encapsulates the bottom chip, the top chip and the bonding wires.

24. (Original) The method of claim 17, wherein the pads are formed on edges of the top surfaces of the chips.

25. (Original) The method of claim 17, wherein the insulator is attached on a central region of the bottom chip, thereby having a width smaller than the bottom chip and the top chip.

26. (Currently amended) A multi-chip module comprising:

a substrate having a plurality of interconnections formed on a top surface thereof;

a lowest chip and at least one top chip sequentially stacked on the top surface, the top chip having an insulating tape attached to a backside thereof, the lowest chip and the top chip each having pads formed thereon, at least one pad being between the lowest chip and the top chip;

an insulator interposed between the chips, the insulator exposing the at least one ~~the~~ pads; and

a first ~~group of~~ bonding wire[[s]] connecting the at least one pad ~~the pads of the lowest chip~~ with a first ~~group of~~ interconnection[[s]] on the substrate,

wherein the insulating tape attached to the backside of the top chip insulates the first ~~group of~~ bonding wire[[s]] from directly contacting the top chip.